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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/633,782	08/07/2000	Gun-Hee Lee	3430-0129P	3862

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EXAMINER

NGUYEN, HOAN C

ART UNIT	PAPER NUMBER
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2871

DATE MAILED: 07/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/633,782

Applicant(s)

LEE ET AL.

Examiner

HOAN C. NGUYEN

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 May 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8, 11-16 and 19-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8, 11-16 and 19-26 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The amendment with new claims 21-26 based on the Response filed on 12/09/2005 have been considered but are moot in view of the new ground(s) of rejection. Therefore, this is Final action.

Claims 9-11 and 17-18 are cancelled.

Election/Restrictions

Applicant's election with traverse of Species B (Figs. 6) in Paper on 05/04/2006 is acknowledged.

Applicant's arguments regarding the restriction requirement have been considered; however, the traversal was on the grounds that there is no serious burden on the Examiner in examining all of claims 1-8, 12-16 and 19-26 together. Applicants point out that there was not a serious burden on the examiner with single reference of Ono et al. (US5847781A), which covers all features (claims 3-4 and 13-14) of the light absorption layers in the two embodiments according to Figs. 5 and 6.

Therefore, the two embodiments are joined due to Ono et al. (US5847781A) covering the light absorption layers in the two embodiments according to Figs. 5 and 6.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 1-2, 12 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Yoshida et al. (US5936693A)** in view of Chang et al. (US6166400), Tadahisa et al. (JP02-02832) and **Kawabe (US6162654A)**.

In regard to claim 1, Yoshida et al. teach (Figs. 2 and 27-31) a liquid crystal display device comprising:

- display panel including a lower layer (substrate 11) at the lowest portion of the display panel and an uppermost layer (substrate 12), positioned above the lowest layer at the uppermost portion of said display panel;
- first substrate 12 forming an uppermost layer of said display panel including
 - a switching element (thin film transistor TFT) on the first substrate and switching element being connected to a gate line 21G and data line; the switching element being a thin film transistor having a gate electrode 15 formed on the first substrate, a gate insulating layer formed on an exposed surface of the first substrate while covering the gate, an active layer on the gate insulating layer over the gate electrode;
 - a pixel electrode 22 over the substrate;
 - a first orientation film 23 formed on pixel electrode

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- a second substrate 12 aligned with the first substrate having a common electrode 31 and a second orientation film 35, the orientation film formed on the common electrode;
- a sealant (seal member SC) for sealing said first and second substrate;
- a liquid crystal layer 13 interposed between the first and second substrates.
- a backlight device disposed beneath said second substrate such that said second substrate is located between said backlight device and said first substrate (col. 6 lines 22-28).

In regard to claim 12, Yoshida et al. teach (Figs. 2 and 27-31) a method of manufacturing a liquid crystal display device, which comprises an array of thin film transistors and an array of pixel electrodes and a backlight device, including:

- forming a gate line GL and a gate electrode 21G on a first substrate said first substrate 11 forming the uppermost layer of a display panel, the gate electrode extending from the gate line;
- forming a gate insulating layer on the exposed surface of the upper substrate while covering the gate line and the gate electrode;
- forming a active layer (semiconductor layer) on the gate insulating layer over the gate electrode;
- forming a data line DL and source and drain electrodes 21S/21D, the source electrode overlapping one end portion of the semiconductor layer, the drain electrode overlapping the other end portion of the semiconductor layer, the

source and drain electrodes 21S/21D spaced apart from each other, the source electrode extending from the data line;

- forming a pixel electrode 22 over gate insulating layer;
- forming a first orientation film 23 over the pixel electrode 22;
- forming a common electrode 31 on a second substrate 12;
- forming a second orientation film 35 on the common electrode;
- aligning the first substrate turned upside down with the second substrate with a gap between the first substrate and the second substrate so that the thin film transistor is also turned upside down and the first orientation film of the first substrate is opposite to the second orientation film of the second substrate;
- sealing the first and second substrate with a sealant SC;
- injecting a liquid crystal between the first substrate and the second substrate;
- positioning said backlight device beneath said second substrate such that said second substrate is located between said backlight device and said substrate (col. 6 lines 22-28).

However, Yoshida et al. fail to disclose

- forming an ohmic contact layer,
- forming a first light absorbing film under the gate electrode
- forming a passivation film over the whole surface of the first substrate while covering the source and drain electrodes, the passivation film having a contact hole on the drain electrode;

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- forming a pixel electrode on the passivation film, the pixel electrode electrically connected with the drain electrode through the contact hole
- forming a color filter on the pixel electrode;
- forming a black matrix BM over the thin film transistor
- forming a first orientation film on the color filters and the black matrices;

Chang et al. teach (Fig. 1) forming the ohmic contact layer 15 between the active layer 13 and source and drain electrodes 16a/b wherein the source electrode overlaps one end portion the active layer and the drain electrode overlaps the other end portion of the active layer for reducing a leakage current (col. 1 lines 43-45 and col. 2 lines 47-50) also according to claim 2.

Tadahisa et al. teach forming a light absorbing film 1 consisting of a-Si under gate electrode 2 and gate line (that is conventionally formed same time with gate electrode) for stable in both characteristics and quality and not affected by a light source by forming a light absorptive layer.

Kawabe (US6162654A) teaches (Figs. 3-8)

- forming a passivation film 22 over the whole surface of the first substrate while covering the source and drain electrodes 20/18, the passivation film having a contact hole on the drain electrode;
- forming a pixel electrode 4 on the passivation film 22, the pixel electrode electrically connected with the drain electrode through the contact hole
- forming a color filter 8 on the pixel electrode;

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- forming a black matrix 9 over the thin film transistor
- forming a first orientation film 10 on the color filters and the black matrices;

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a liquid crystal display device as Yoshida et al. disclosed with (1) forming the ohmic contact layer between the active layer and source and drain electrodes wherein the source electrode overlaps one end portion the active layer and the drain electrode overlaps the other end portion of the active layer for reducing a leakage current as taught by Chang et al. (col. 1 lines 43-45 and col. 2 lines 47-50); (2) forming a first light absorbing film between the first substrate and the gate electrode, gate line for stable in both characteristics and quality and not affected by a back light by forming a light absorptive layer as taught by Tadahisa et al.; (3) forming a passivation film over the whole surface of the first substrate, a pixel electrode on the passivation film, a color filter on the pixel electrode and a black matrix over the thin film transistor for high quality display as taught by Kawabe (col. 1 lines 7-9 and col. 2 lines 34-36).

2. Claims 3-8, 13-16 and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Yoshida et al. (US5936693A)** in view of Chang et al. (US6166400), Tadahisa et al. (JP02-02832) and **Kawabe (US6162654A)** as applied to claims 1-2 and 12 and in further view of Ono et al. (US5847781A).

Yoshida et al. also teach the pixel electrode and common electrode made of indium tin oxide (ITO), which is transparent material as claims 8, 15-16, 20-20 cited.

Yoshida et al. fail to disclose the features of claims 3-4, 5-6, 13-14 and 21-23.

Ono et al. teach (Figs. 3 and 7, col. 7 lines 5-16) a liquid crystal display device further comprising a light absorbing film AS formed under the active layer d0 and under the source electrode or data line DL or drain electrode SD1 for reducing reflecting or scattering from source and drain electrodes or data lines, and therefore resulting in dark display.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a liquid crystal display device as Yoshida et al. disclosed with forming a second light absorbing film between the active layer and the gate insulating layer for reducing reflecting or scattering from source, drain electrodes or data lines, and therefore resulting in dark display as taught by Ono et al. (col. 7 lines 5-16).

3. Claims 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Yoshida et al. (US5936693A)** in view of Chang et al. (US6166400), Tadahisa et al. (JP02-02832) and **Kawabe (US6162654A)** as applied to claims 1-2 and 12 and in further view of Ono et al. (US5847781A) as applied to claims 3-4, 6, 13-14 and 21-23 and in further view of **Oyama et al. (US5976684A)**.

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Yoshida et al. fail to disclose the features of claims 24-26.

Oyama et al. teach a titanium nitride film has a proper optical constant in a visible light region and well matches when a silica film is used as the low refractive index film. With a film thickness of about 10 nm, a low reflectance and a proper light absorption can be obtained.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a liquid crystal display device as Yoshida et al. disclosed with the light absorption films comprising a low reflectance material of titanium nitride film for high durability or low cost (col. 6 lines 13-18).

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

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extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HOAN C. NGUYEN whose telephone number is (571) 272-2296. The examiner can normally be reached on MONDAY-THURSDAY:8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HOAN C. NGUYEN
Examiner
Art Unit 2871

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ANDREW SCHECHTER
PRIMARY EXAMINER